REMARKS

Claims 22 and 57 are amended. Claims 64 and 65 are added. Claims 12, 13, 16, 21-23, 47, 53 and 56-65 are in the application for consideration.

Claim 22 stand rejected under 35 U.S.C. § 112 first and second paragraphs. Without admitting to the propriety of the Examiner's action, the allegedly offending language has been removed from claim 22. Accordingly, these rejections should be withdrawn.

Claim 22 is amended to recite that the subject etching of material of the conductive plug is from an entirety of the plug uppermost surface. This same limitation is found in allowed claim 62. Claim 22 additionally recites that the first uppermost surface of the plug has a width which terminates over respective conductive lines of the pair of conductive lines.

Crotti discloses neither of these features. Accordingly, Crotti could not impliedly or otherwise suggest that which Applicant recites in the independent claim 22 combination. Accordingly, claim 22 should be allowed, and action to that end is requested.

Dependent claim 23 should be allowed as depending from an allowable base claim, and for its own recited features which are neither shown nor suggested in the cited art. Action to that end is requested.

Claim 57 is amended to insert an indent/tab which was mistakenly not included in Applicant's last filed response. Entry of the same is requested.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: 10-31-02

By: 

Mark S. Matkin
Reg. No. 32,268

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/909,111
Filing Date ..... July 18, 2001
Inventor ..... Mark Fischer, et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 1765
Examiner ..... Duy Deo
Attorney's Docket No. MI22-1777
Title: Semiconductor Processing Methods of Forming a Conductive Projection and Methods of Increasing Alignment Tolerances

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO OCTOBER 16, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

22. (Four Times Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface over the node location having ~~a generally uniform surface and having~~ a width terminating over respective conductive lines of the pair of conductive lines; and

etching material of the conductive plug ~~through the first~~ from an entirety of the plug uppermost surface to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug.

57. (Twice Amended) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

_____forming insulative material over the conductive contact projections after the etching;

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections; and

wherein at least the one projection has an uppermost surface which is substantially planar immediately prior to the etching of the one projection.

New claims 64 and 65 are added.

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